IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/679,623	§	Examiner: Vidwan, J.
Filed: October 6, 2003	§	Group/Art Unit: 2182
Inventor(s):	§	Atty. Dkt. No: 5500-92201
René Röllig et al.	§	
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Title: METHOD AND DEVICE FOR HANDLING SMBUS MESSAGES	§	
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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Erik A. Heter
Printed Name

/Erik A. Heter/ 7/6/09
Signature Date

REQUEST FOR PRE-APPEAL BRIEF REVIEW

ATTN: BOX AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

REMARKS

The Examiner maintains the 35 U.S.C. § 103(a) rejection of claims 1, 6-10, 15-19, 28-31 and 96 as being unpatentable over Stancil in view of Luke and Steely. Applicant respectfully submits that this rejection is erroneous for at least the following reasons.

In the final office action response of May 5, 2009, Applicant argued that the Stancil in view of Luke and Steely fails to teach or suggest all of the elements of the independent claims. Applicant submits that Stancil in view of Luke and Steely fails to teach "a finite-state machine configured to receive and interpret the instructions read by said instruction fetch unit and manage the data transfer between the SMBus interface and a register set in compliance with said instructions read from said memory." In the Advisory Action of June 2, 2009, the Examiner contends the following:

> Stancili's state machine alone would not "interpret" the instructions read from the instruction fetch unit in part because Stancil does not teach IFU. It is the position of the Examiner that the State machine taught by Stancil functions as a logic that would be inherently capable of reading and processing (interpret) instructions read through the instruction fetch unit as combined by the secondary references of Luke and steele. The Op code of Luke functions as an instruction fetch unit as it stores the current instruction for the sequencer commands that are addressed by the program counter. Further, the sequencer coupled with the op code (Col. 9, Lines 14-20) retrieve instructions from the external memory. Therefore it is the position of the Examiner that collectively the op-code and sequencer 46 perform the functions that of an instruction fetch unit as addressed in the claimed limitation. (Emphasis added).

Applicant agrees with the Examiner's statement that Stancil's state machine alone would not interpret instructions read from an instruction fetch unit, and further agrees that Stancil fails to teach an instruction fetch unit (IFU). However, Applicant respectfully disagrees with the Examiner's statement that the "[s]tate machine taught by Stancil ... would be inherently capable of reading and processing (interpret) instructions." Applicant submits that the Examiner provides no basis, in either the advisory action or the final office action of May 5, 2009, for the contention that the ability to interpret instructions is inherent. With regard to inherency, MPEP 2112 states, in pertinent part:

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the

allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original)

Despite contending that the state machine of Stancil is "inherently capable of reading and processing (interpret) instructions," the Examiner has provided no basis in fact and/or technical reasoning as to why this allegedly inherent capability necessarily flows from the applied prior art, per the requirements of MPEP 2112 noted above. With respect to elements 112 and 116 of Stancil (which the Examiner reads on Applicant's recited "finite-state machine"), Stancil states the following in col. 4, lines 14-32:

> FIGS. 2-5 provide further detail regarding SMBus-to-JTAG emulator 110 pertaining to how the emulator converts between SMBus and JTAG. A more detailed block diagram of emulator 110 is shown in FIG. 2. As shown therein, the emulator 110 preferably comprises an SMBUs state machine 112, an SMBus packet decoder/encoder 114 and a JTAG interface logic state machine 116. The SMBus state machine 112 comprises logic that receives SMBus packets from the host test system 102 and, with the help of the SMBus packet decoder/encoder 114, extracts the information from the packets necessary for the JTAG logic 122. The decoder/encoder 114 then creates JTAG-compliant communications that are sent to the JTAG logic 122 associated with the DUT 120 under the control of the JTAG interface logic state machine 116. Similarly, JTAG communications from the JTAG logic 122 are received by state machine 116, decoded by decoder/encoder 114 and are converted to SMBus-compliant packets by decoder/encoder 114 and provided to the host test system 102 under the control of the SMBus state machine 112. (Emphasis added).

Nothing in the above citation teaches, much less suggests, that either of state machines 112 or 116 is "inherently capable of reading and processing [interpreting] instructions." Absent any teaching or suggestion in the above quotation, and absent any technical reasoning as to why the recited combination of features is inherent, Applicant submits that the alleged inherency has not been established.

Applicant further notes that other than the quotation above, Stancil provides no additional discussion regarding state machines 112 and 116. Thus, the Stancil does not provide any teaching or suggestion that state machines 112 and/or 116 "manage the data transfer ... in compliance with said instructions read from said memory." Furthermore, neither Luke nor Steely provides any teaching or suggestion that, taken singly or in combination with the other references, results in this combination of features. Thus, lacking any additional teachings regarding state

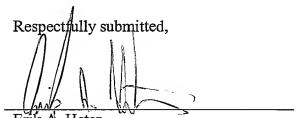
machines 112 and/or 116, as well as any technical reasoning as to why either or both of these state machines are "inherently capable of reading and processing [interpreting] instructions," much less any teaching that state machines 112 and/or 116 are "configured to ... manage the data transfer between the SMBus interface and a register set in compliance with said instructions read from said memory," it follows that Stancil in view of Luke and Steely fail to teach or suggest all of the elements of the independent claims, including "a finite-state machine configured to receive and interpret the instructions read by said instruction fetch unit and manage the data transfer between the SMBus interface and a register set in compliance with said instructions read from said memory." Accordingly, Applicant submits that a case of obviousness has not been established, and the respectfully requests reversal of the Examiner's rejection.

CONCLUSION

Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-92201/EAH.

Respectfully submitted,



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